



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/702,363	11/06/2003	Ravi Pratap Singh	A0312.70461US00	8515
7590	03/27/2006		EXAMINER	
William R. McClellan Wolf, Greenfield & Sacks, P.C. 600 Atlantic Avenue Boston, MA 02210			CODY, DILLON J	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/702,363	SINGH ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Dillon Cody	2183	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 06 November 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 November 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

1. Claims 1-30 are pending.

***Papers Filed***

2. Examiner acknowledges receipt of claims, disclosure, and informal drawings, all filed 6 November 2003 and declaration filed 10 May 2004.

***Title***

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

***Drawings***

4. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because formal drawings have not yet been submitted. Applicant is advised to employ the services of a competent patent draftsman outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

***Claim Objections***

5. Claims 1 and 17 are objected to because of the following informalities:

Claim 1, line 12: "and" should follow the semicolon of step C in order to explicitly require all four steps of the method to be present

Claim 17, line 7: "to" should follow "response"

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Parthasarathy (U.S. Patent No. 6,671,799).

8. As per claim 1, Parthasarathy discloses a method for issuing instructions in a processor having a pipeline, comprising:

(a) providing a loop buffer (Fig. 2 loop buffer 212) for holding program loop instructions and a register file (Fig. 2 loop setup 222) for holding speculative and architectural loop control parameters (Col. 6 lines 65-67); *The examiner asserts that any parameters stored in register file 222 which are not part of an active loop are speculative, and those which are a part of an active loop are architectural.*

(b) in response to decoding of a first loop setup instruction, marking a first entry in the register file as a current entry and writing in the first entry loop control parameters represented in the first loop setup instruction; (Col. 7 lines 49-57) *The examiner asserts that while loop conditions are written to a set of registers, those registers must be selected before being written to and constitute current register entries.*

(c) marking the current entry in the register file as an architectural entry in response to the first loop setup instruction being committed in the pipeline; (Col. 7 lines 49-57 and col. 5 lines 31-33) *The examiner asserts that when a loop begins and the first instruction is matched to the loop start register (LSR0, 1 or 2), the setup is committed, the loop is begun and the selected loop start register and its associated loop stop and loop count (LER and LCR) registers are considered to be architectural registers.*

(d) sending a loop bottom indicator down the pipeline with a loop bottom instruction. *The examiner asserts that Parthasarathy's invention inherently sends a loop bottom indicator down the pipeline since one of registers LCR0, LCR1 and LCR2 contains the active loop count. If no loop bottom indicator arrived at the architectural registers, the count would never decrement and the loop would never exit, causing undesired operation.*

9. As per claim 2, Parthasarathy discloses a method as defined in claim 1, further comprising decrementing a loop count in the architectural entry in the register file in

Art Unit: 2183

response to the loop bottom instruction being committed in the pipeline. (Col. 8 lines 57-60)

10. As per claim 3, Parthasarathy discloses a method as defined in claim 1, further comprising issuing instructions of the program loop according to the loop control parameters in the current entry in the register file. (Col. 6 lines 27-39)

11. As per claim 4, Parthasarathy discloses a method as defined in claim 1, wherein the register file has at least three entries. (Fig. 3 registers LER and LSR 0-2)

12. As per claim 5, Parthasarathy discloses a method as defined in claim 4, further comprising generating a current pointer to the current entry in the register file and generating an architectural pointer to the architectural entry in the register file. *The examiner asserts that any time a set of loop registers is updated, information must be decoded to label it as a current register. The current registers are labeled as such by the incoming Loop Setup signals in Fig. 3 (Col. 7 lines 49-57). The architectural entry is determined to be so by matching the PC with the addresses stored in the loop registers. (Col. 5 lines 31-33)*

13. As per claim 6, Parthasarathy discloses a method as defined in claim 5, further comprising incrementing the current pointer to a second entry in the register file in response to decoding of a second loop setup instruction and writing in the second entry

loop control parameters represented in the second loop setup instruction. *The examiner asserts that a second entry is inherently selected by any second loop set up instruction (Col. 7 lines 49-57). Once a loop register is selected, it becomes current as it is being written.*

14. As per claim 7, Parthasarathy discloses a method as defined in claim 6, further comprising incrementing the architectural pointer to the second entry in the register file in response to the second loop setup instruction being committed. *The examiner asserts that when a loop begins and the first instruction is matched to the loop start register (LSR0, 1 or 2), the setup is committed, the loop is begun and the selected loop start register and it's associated loop stop and loop count (LER and LCR) registers are considered to be architectural registers.*

15. As per claim 8, Parthasarathy discloses a method as defined in claim 6, further comprising moving the current pointer to a location of the architectural pointer in response to an interrupt or a pipeline abort. (Col. 6 lines 54-66) *The examiner asserts that a loop flush constitutes an interrupt of processing. When such a flush happens, the loop setup registers are consulted, making them current registers.*

16. As per claim 9, Parthasarathy discloses a method as defined in claim 1, wherein step (b) comprises writing a loop top address to a loop top register, writing a loop

bottom address to a loop bottom register and writing a loop count to a loop count register. (Col. 1 lines 34-36 and Col. 7 lines 49-57)

17. As per claim 10, Parthasarathy discloses a method as defined in claim 9, further comprising comparing a current instruction address with the loop top address to determine a loop top match and comparing the current instruction address with the loop bottom address to determine a loop bottom match. (Col. 7 lines 19-48)

18. As per claim 11, Parthasarathy discloses a method as defined in claim 10, further comprising writing a temporary loop count in a temporary loop count register and decrementing the temporary loop count on each loop bottom match. *The examiner asserts that the LCR is a temporary loop count register. The value held therein remains at a value for a limited amount of time before being decremented to a new value.* (Col. 8 lines 57-60)

19. As per claim 12, Parthasarathy discloses a method as defined in claim 11, further comprising exiting the program loop when the temporary loop count has decremented to zero. (Col. 5 lines 46-60)

20. As per claim 13, Parthasarathy discloses a method as defined in claim 1, further comprising stalling a loop setup instruction when the register file does not have an available entry. *The examiner asserts that a loop setup instruction must inherently be*



*stalled if no destination registers are available. If the setup instruction was not stalled, the processor may break from the current loop before the count register reached zero, causing undesired operation.*

21. As per claim 14, Parthasarathy discloses a method as defined in claim 1, wherein instructions are issued without sending the loop control parameters down the pipeline. *The examiner asserts that the loop control parameters reside in the loop control registers (LSR, LER, LCR) and do not travel down the pipeline with issued instructions.*

22. As per claim 15, Parthasarathy discloses a method as defined in claim 1, further comprising writing instructions of the program loop to the loop buffer on a first iteration of the program loop. (Col. 6 lines 27-30)

23. As per claim 16, Parthasarathy discloses a method for controlling a program loop in a processor having a pipeline, comprising:

(a) providing a loop buffer (Fig. 2 loop buffer 212) for holding program loop instructions and a register file (Fig. 2 loop setup 222) having at least three entries for holding speculative and architectural loop control parameters (Col. 6 lines 65-67); *The examiner asserts that any parameters stored in register file 222 which are not part of an active loop are speculative, and those which are a part of an active loop are architectural.*

(b) marking a first entry in the register file as a current entry in response to decoding of a first loop setup instruction and writing in the first entry loop control parameters represented in the first loop setup instruction; (Col. 7 lines 49-57) *The examiner asserts that while loop conditions are written to a set of registers, those registers must be selected before being written to and constitute current register entries.*

and (c) marking the first entry in the register file as an architectural entry in response to the first loop setup instruction being committed in the pipeline. (Col. 7 lines 49-57 and col. 5 lines 31-33) *The examiner asserts that when a loop begins and the first instruction is matched to the loop start register (LSR0, 1 or 2), the setup is committed, the loop is begun and the selected loop start register and it's associated loop stop and loop count (LER and LCR) registers are considered to be architectural registers.*

24. As per claim 17, Parthasarathy discloses an apparatus for issuing instructions in a processor having a pipeline, comprising:

a loop buffer for holding program loop instructions; (Fig. 2 loop buffer 212)

a register file having at least three entries for holding speculative and architectural loop control parameters; (Fig. 2 loop setup 222) *The examiner asserts that any parameters stored in register file 222 which are not part of an active loop are speculative, and those which are a part of an active loop are architectural.*

and a controller including means for marking a first entry in the register file as a current entry in response decoding of a first loop setup instruction (Col. 7 lines 49-57)

and for writing in the first entry loop control parameters represented in the first loop setup instruction, and means for marking the current entry in the register file as an architectural entry in response to the first loop setup instruction being committed. (Col. 7 lines 49-57 and col. 5 lines 31-33) *The examiner asserts that while loop conditions are written to a set of registers, those registers must be selected before being written to and constitute current register entries. When a loop begins and the first instruction is matched to the loop start register (LSR0, 1 or 2), the setup is committed, the loop is begun and the selected loop start register and it's associated loop stop and loop count (LER and LCR) registers are considered to be architectural registers.*

25. As per claim 18, Parthasarathy discloses an apparatus as defined in claim 17, wherein the controller further comprises means for issuing instructions of the program loop according to the loop control parameters in the current entry in the register file (Col. 6 lines 27-39), sending a loop bottom indicator down the pipeline with a loop bottom instruction, and decrementing a loop count in the architectural entry in the register file in response to the loop bottom instruction being committed in the pipeline. (Col. 8 lines 57-60) *The examiner asserts that Parthasarathy's invention inherently sends a loop bottom indicator down the pipeline since one of registers LCR0, LCR1 and LCR2 contains the active loop count. If no loop bottom indicator arrived at the architectural registers, the count would never decrement and the loop would never exit, causing undesired operation.*

Art Unit: 2183

26. As per claim 19, Parthasarathy discloses an apparatus as defined in claim 18, wherein the controller further comprises means for marking a second entry in the register file as the current entry in response to decoding of a second loop setup instruction and for writing in the second entry loop control parameters represented in the second loop setup instruction, and means for marking the second entry in the register file as the architectural entry in response to the second loop setup instruction being committed. *The examiner asserts that a second entry is inherently selected by any second loop set up instruction (Col. 7 lines 49-57). Once a loop register is selected, it becomes current as it is being written. The examiner asserts that when a loop begins and the first instruction is matched to the loop start register (LSR0, 1 or 2), the setup is committed, the loop is begun and the selected loop start register and it's associated loop stop and loop count (LER and LCR) registers are considered to be architectural registers.*

27. As per claim 20, Parthasarathy discloses an apparatus as defined in claim 17, wherein each entry in the register file comprises a loop top register for holding a loop top address, a loop bottom register for holding a loop bottom address and a loop count register for holding a loop count. (Col. 1 lines 34-36 and Col. 7 lines 49-57)

28. As per claim 21, Parthasarathy discloses an apparatus performing the method of claim 10. Therefore, claim 21 is rejected under the same grounds as claim 10 listed above.

29. As per claim 22, Parthasarathy discloses an apparatus performing the method of claim 11. Therefore, claim 22 is rejected under the same grounds as claim 11 listed above.

30. As per claim 23, Parthasarathy discloses an apparatus performing the method of claim 12. Therefore, claim 23 is rejected under the same grounds as claim 12 listed above.

31. As per claim 24, Parthasarathy discloses an apparatus performing the method of claim 13. Therefore, claim 24 is rejected under the same grounds as claim 13 listed above.

32. As per claim 25, Parthasarathy discloses an apparatus performing the method of claim 14. Therefore, claim 25 is rejected under the same grounds as claim 14 listed above.

33. As per claim 26, Parthasarathy discloses an apparatus performing the method of claim 15. Therefore, claim 26 is rejected under the same grounds as claim 15 listed above.

34. As per claim 27, Parthasarathy discloses an apparatus performing the method of claim 5. Therefore, claim 27 is rejected under the same grounds as claim 5 listed above.

35. As per claim 28, Parthasarathy discloses an apparatus performing the method of claim 6. Therefore, claim 28 is rejected under the same grounds as claim 6 listed above.

36. As per claim 29, Parthasarathy discloses an apparatus performing the method of claim 7. Therefore, claim 29 is rejected under the same grounds as claim 7 listed above.

37. As per claim 30, Parthasarathy discloses an apparatus performing the method of claim 8. Therefore, claim 30 is rejected under the same grounds as claim 8 listed above.

### ***Conclusion***

38. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Inoue et al. (U.S. Publication No. 2002/0078333) disclose a hardware loop system comprising "early" registers in addition to architectural registers for storing loop control parameters.

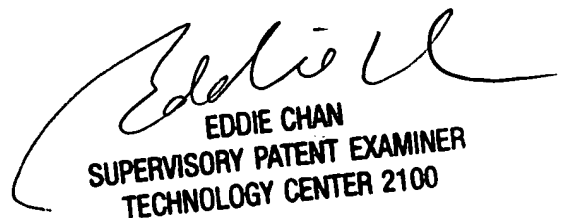
39. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

  
EDDIE CHAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100